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Sidewall Crystalline Orientation Effect of Post-treatments for a Replacement Metal Gate Bulk Fin Field Effect Transistor

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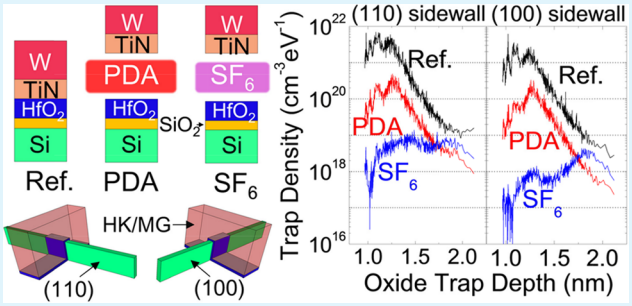
ABSTRACT: The crystalline orientation effect is investigated for post-treatments of a replacement metal gate (RMG) p-type bulk fin field effect transistor (FinFET). After post-deposition annealing (PDA) and SF_6 plasma treatment, the hole mobility is improved. From low-frequency noise analysis, reduction of the trap density and noise level is observed in PDA- and SF_6-plasma-treated devices. (100) sidewall-oriented FinFETs show a lower noise level because of fewer interface traps compared to (110) sidewall-oriented devices. SF_6 plasma affects the interface traps, whereas PDA relatively more affects bulk oxide traps for RMG high-*k* last FinFET.



KEYWORDS: *FinFET, crystalline orientation, low-frequency noise, replacement metal gate, post-deposition annealing, SF_6 plasma*

1. INTRODUCTION

The high-*k*/metal gate (HK/MG) has played an important role in the downscaling of complementary metal−oxide semiconductor technology. Recently, the replacement metal gate (RMG) scheme has been introduced.[1,2] In the RMG high-*k* last scheme, a dummy poly-Si/SiO_2 gate stack is etched away and replaced by HK/MG after junction formation and dopant activation. Therefore, an aggressive thermal budget for the HK/MG stacks can be avoided using RMG integration. However, the oxide etching and following HK/MG stack induce additional interface states and degrade the device performance.[3] To improve the quality of the RMG HK/MG stack, additional post-treatment is necessary such as post-deposition annealing (PDA) or SF_6 plasma treatment.[4,5]

Implementation of the RMG scheme for a fin field effect transistor (FinFET) is more complicated. Because of the three-dimensional channel structure of a FinFET, the surface property of the fin sidewall is different from that of the top surface of the fin. The etching process for fin formation induces higher surface roughness and interfacial states on fin sidewalls.[6] Additionally, FinFETs can be fabricated with either a (110) or (100) crystalline orientation of the sidewall surface. Because carrier transport on the sidewall becomes dominant at narrow fin width, the study of the fin sidewall orientation is very important.[7]

In this paper, the performance improvement of high-*k* last p-type bulk FinFET using PDA and SF_6 plasma treatment is investigated based on the different crystalline orientations of the fin sidewall. Using low-frequency noise analysis, the noise level and trap density profile are compared for each post-treatment scheme.

2. EXPERIMENTAL SECTION

Two different post-treated high-*k* last FinFETs (PDA and SF_6 plasma) are prepared with nothing-treated high-*k* last FinFET references for each of the (110) and (100) sidewall orientations. The fin channel structure is patterned on a (100) surface-oriented 300 mm silicon wafer and doped before a Si/SiO_2 dummy gate stack deposition. (100) sidewall-surface-oriented FinFET is fabricated by 45° rotation of (110) sidewall-surface-oriented FinFET, as shown in Figure 1. After halo and

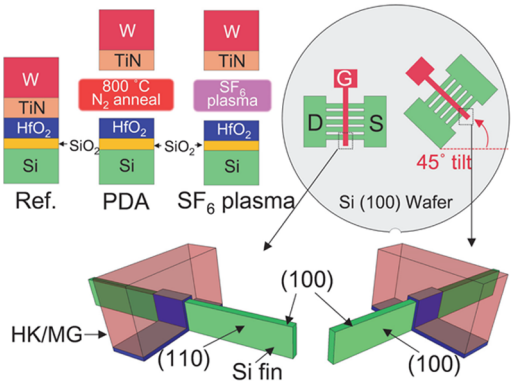


Figure 1. Schematics of RMG high-*k* last gate stacks for bulk FinFET with different fin sidewall orientations. Three different post-treatment schemes (untreated reference, PDA, and SF_6 plasma) are used after HfO_2 deposition.

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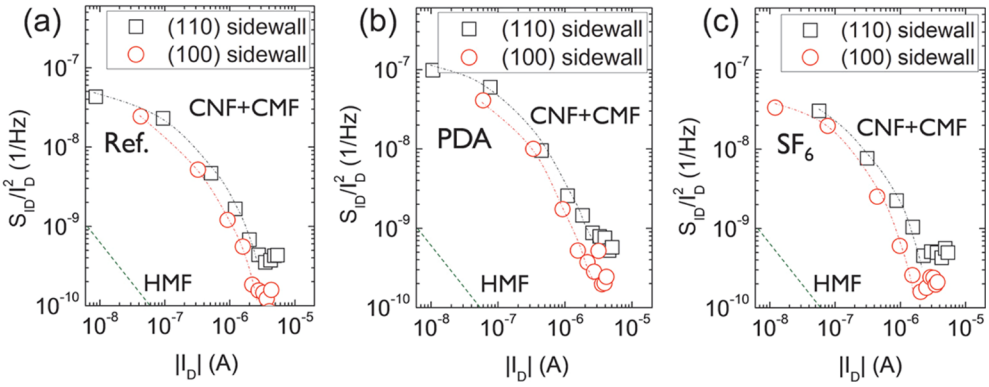

Figure 2. Normalized drain current noise power spectral density at 50 Hz and V_D = −50 mV for (a) untreated reference and (b) PDA- and (c) SF_6-plasma-treated FinFETs with different sidewall surface orientations. Low-frequency noise behavior is well matched with the CNF+CMF model. (100) sidewall-surface-oriented FinFETs show lower noise levels for all post-treatment schemes.

Table 1. Summary of Device Parameters According to the Different Post-treatment Schemes and Fin Sidewall Orientations for W_{fin} = 20 nm, H_{fin} = 30 nm, and L_G = 1 μm at 50 Hz

	sidewall orientation, post-treatment					
	(110), reference	(110), PDA	(110), SF_6 plasma	(100), reference	(100), PDA	(100), SF_6 plasma
peak of effective mobility ($cm^2/V{\cdot}s$)	146	151	156	80	91	108
$AS_{VG}f$ ($\mu m^2{\cdot}V^2$)	6.36×10^{-10}	1.76×10^{-10}	2.63×10^{-10}	2.68×10^{-10}	1.26×10^{-10}	1.38×10^{-10}
N_t ($cm^{-3}{\cdot}eV^{-1}$)	8.04×10^{19}	1.91×10^{19}	2.27×10^{19}	3.38×10^{19}	1.37×10^{19}	1.50×10^{19}
α (V·s/C)	1.21×10^{4}	2.22×10^{4}	1.44×10^{5}	1.7×10^{4}	3.25×10^{4}	1.53×10^{5}
EOT (nm)	0.77	0.83	0.83	0.70	0.70	0.73

source/drain (S/D) extensions are doped and spacers are formed, the RMG module is implemented. First, the Si/SiO_2 dummy gate stack is chemically etched. Then, the interfacial layer oxide is grown using O_3 oxidation and a 1.8 nm HfO_2 high-k layer is deposited using atomic layer deposition. For improvement of the HK/MG stack, PDA at 800 °C during 1 s or radio-frequency-power-induced SF_6 plasma during 9 min is employed. SF_6 plasma with argon as an inert gas was optimized to increase the number of ions reaching the bottom of the narrow trench effectively. Finally, gate metal is deposited, and S/D silicidation is carried out. In this study, the device dimensions are fixed as fin width W_{fin} = 20 nm, fin height H_{fin} = 30 nm, and gate length L_G = 1 μm.

A BTA 9812 noise analyzer is used for the low-frequency noise measurement. All noise measurements were carried out under V_D = −50 mV for the linear operation regime.

3. RESULTS AND DISCUSSION

In Figure 2, the sidewall orientation comparisons of normalized drain current noise power spectral density S_{ID}/I_D^2 at 50 Hz are shown for the untreated reference (Figure 2a) and PDA-treated (Figure 2b) and SF_6-plasma-treated (Figure 2c) FinFETs. The low-frequency noise mechanism can be modeled by two well-known approaches: (i) the carrier number + correlated mobility fluctuation (CNF+CMF) model based on carrier trapping and detrapping near the dielectric/semiconductor interface and associated mobility fluctuations due to Coulomb scattering. In the CNF+CMF model, S_{ID}/I_D^2 mainly follows $(g_m/I_D)^2$ shape[8,9]

$$\frac{S_{ID}}{I_D^2} = (1 + \alpha\mu_{eff}C_{ox}I_D/g_m)^2 S_{Vfb}\left(\frac{g_m}{I_D}\right)^2 \quad (1)$$

where α is the Coulomb scattering parameter relevant to mobility fluctuation (V·s/C), μ_{eff} the effective mobility ($cm^2/V{\cdot}s$), C_{ox} the oxide capacitance per unit area (F/cm^2), g_m the transconductance [$=\delta I_D/\delta V_G$ (A/V)], S_{Vfb} the flat-band voltage power spectrum (V^2/Hz). In contrast, (ii) the Hooge mobility fluctuation (HMF) model is based on the carrier mobility fluctuation by phonon interaction. S_{ID}/I_D^2 is proportional to I_D^{-1} in the HMF model[8,9]

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{N_c f} \propto \frac{1}{I_D} \quad (2)$$

where α_H is the Hooge constant and N_c the total carrier number. Figure 2 clearly shows that the low-frequency noise of RMG high-k last FinFETs is based on the CNF+CMF model affected by carrier trapping/detrapping events.

For all cases in Figure 2, the (100) sidewall shows lower S_{ID}/I_D^2 trends due to relatively lower interface traps on the (100) sidewall surface. Because the number of Si atoms per unit area on the (110) surface is approximately 1.4 times higher than that on the (100) surface, (110) sidewall-oriented FinFETs have a higher density of dangling bonds than (100) sidewall-oriented FinFETs, resulting in an increased trap density near the Si/SiO_2 interface.[10,11]

Because the low-frequency noise mechanism of RMG FinFETs originates from carrier trapping/detrapping, the tunneling depth dependence of the trap density can be calculated. The oxide trap depth z is converted from the frequency information according to[9,12,13]

$$z = \lambda \ln\left(\frac{1}{2\pi f \tau_0}\right) \quad (3)$$

with τ_0 the tunneling time constant, which is approximately 10^{-10} s, and λ the oxide tunneling distance at approximately

10^{-8} cm. The oxide trap density N_t can be calculated from S_{Vfb} affected by charge trapping and detrapping based on the tunneling process into the gate oxide[8]

$$S_{Vfb} = \frac{q^2 k_B T \lambda N_t}{f W L C_{ox}^{\ 2}} \quad (4)$$

where q is the electric charge, k_B the Boltzmann constant, T the temperature, f the frequency, W the total channel width (W_{fin} + $2H_{fin}$), and L the channel length.

The N_t values are calculated by fitting eqs 1 and 4 to S_{ID}/I_D^2. μ_{eff} and C_{ox} were estimated using the split $C-V$ method.[14] The device parameters for the fitting are shown in Table 1. As shown in Table 1, higher hole effective mobility in the (110) fin sidewall surface is generally shown compared to the (100) sidewall surface. Higher hole mobility in the (110) surface than the (100) surface has been reported.[7,15−17] Generally, the (110) silicon surface orientation has a lighter hole effective mass than (100) because of the hole effective mass anisotropy in different silicon surface orientations, and it makes the effective mobility higher. In the FinFET with a narrow fin width, the sidewall surface orientation is dominant for carrier transport. Thus, the FinFET with the (110) sidewall surface has higher mobility than that with the (100) sidewall surface orientation.

Figure 3 shows the oxide trap density profiles as a function of the oxide trap depth at $V_G = V_T$. For both (110) and (100)

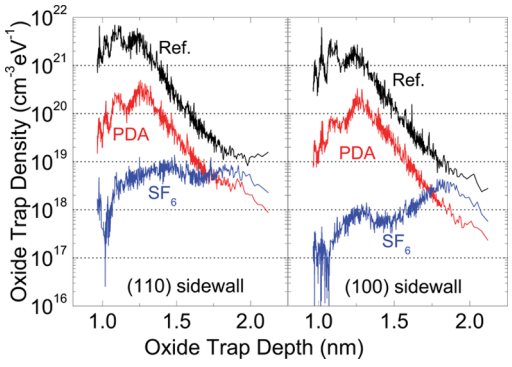

Figure 3. Trap density profile as a function of the trap depth at $V_G = V_T$. SF_6-plasma-treated devices have the lowest trap density near the interface, whereas PDA-treated devices have lower bulk oxide traps at high oxide trap depth. Each post-treatment condition of (100) sidewall FinFETs has lower trap density profiles compared to those of (110) sidewall FinFETs.

sidewall-oriented FinFETs, PDA- and SF_6-plasma-treated devices have reduced trap densities compared to the references. It is clearly shown that the SF_6-plasma-treated devices show lower traps near the interface. In contrast, PDA-treated devices show lower traps in the bulk oxide region. PDA-treated devices show that the high trap density near the interface exponentially decreases in the bulk oxide region, whereas the trap densities of SF_6-plasma-treated devices gradually increase or become saturated as the trap depth increased.

Previously, the effect of PDA and SF_6 plasma treatments has been reported for planar devices. The PDA treatment reduces the oxygen vacancies in the HfO_2 layer.[18,19] During PDA treatment, the oxygen vacancies are passivated by nitrogen in bulk oxide. In the study of SF_6 plasma treatment, interface trap passivation by Hf−F and Si−F bonds has been shown.[20,21]

In Figure 3, the SF_6-plasma-treated device shows approximately 1 decade difference between (110) and (100) sidewall-oriented FinFETs near the interface, whereas reference and PDA-treated devices show relatively small differences (2−3 times). It seems that the SF_6 plasma treatment gives a more interface state dominant effect compared to the PDA treatment. Near the interface, the trap density profile depends on the interface traps. Higher dangling bonds on the (110) sidewall induce higher interface traps compared to the (100) sidewall surface. Thus, the higher sidewall surface orientation dependence of the SF_6 plasma treatment near the interface means more interface trap passivation effect of the SF_6 plasma treatment for RMG FinFET.

Figure 4a shows bulk oxide trap densities estimated at 50 Hz and different sidewall surface orientations for each post-

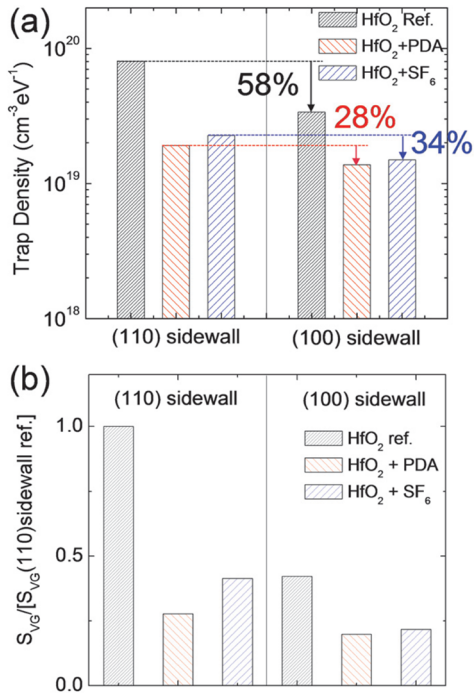

Figure 4. (a) Trap density at 50 Hz and (b) input-referred voltage noise normalized by the (110) reference. PDA and SF_6 plasma treatment reduces the traps and noise level. Both parts a and b shows that the SF_6 plasma treatment is more surface-orientation-dependent.

treatment scheme. At the (100) sidewall surface, the untreated reference shows 58% reduced trap density compared to the (110) sidewall-oriented one. For PDA and SF_6 plasma treatment, 28% and 34% reductions are shown respectively at (100) sidewall FinFETs. Even though the untreated reference shows the most reduced trap density at the (100) sidewall, it still has the highest trap density compared to the PDA and SF_6 plasma treatment options at the same sidewall orientation.

In Figure 4b, the input-referred noise S_{VG} ($S_{VG} = S_{ID}/g_m^2$) is compared at 50 Hz and $V_G = V_T$. Each S_{VG} is normalized by the date for the untreated reference with the (110) sidewall for quantitative comparison. All (100) sidewall-oriented FinFETs show reduced S_{VG} values compared to (110) sidewall devices. Whereas the SF_6-plasma-treated device has 1.51 times higher S_{VG} than the PDA-treated one at the (110) sidewall surface, it is 1.09 times higher for the SF_6 plasma compared to the PDA option at the (100) sidewall surface. The crystalline orientation of the fin sidewall seems more effective for SF_6 plasma post-treatment, which means that SF_6 plasma affects more interface traps. At the (100) sidewall FinFET, the SF_6 plasma post-

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treatment option has the advantage of low-frequency noise and interface trap compared to the other options and improved low-frequency noise similar to PDA-treated FinFETs.

4. CONCLUSION

In conclusion, PDA and SF_6 plasma post-treatments have been studied for the RMG high-*k* last p-type bulk FinFETs according to the different sidewall orientations. In the RMG high-*k* scheme, PDA and SF_6 post-treatments reduce the low-frequency noise and trap density. (100) sidewall-surface-oriented devices show lower noise and trap density for all post-treatment schemes compared to (110) sidewall FinFETs. The SF_6 plasma treatment relatively more affects the interface traps, whereas PDA more affects bulk oxide traps for the RMG HK/MG stack.

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Notes

The authors declare no competing financial interest.

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